VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD
B.E. (CSE: CBCS) III-Semester Supplementary Examinations, May/June-2018
Logic & Switching Theory

Time: 3 hours   Max. Marks: 70

Note: Answer ALL questions in Part-A and any FIVE from Part-B

Part-A (10 × 2 = 20 Marks)

1. Simplify the function Y = AB+A(B+C)+B(B+C) using Boolean theorems.

2. Show that (B+D)(A+D)(B+C)(A+C)=AB+CD.

3. Implement NOR gate using 2:1 Multiplexer.

4. Simplify each of the following function and implement with NAND gates.
   $F = AC^1 + ACE + ACE^1 + ACD + ADE$

5. Design a single bit comparator.

6. Implement full subtractor using De Multiplexer.

7. What is 'race around'(unstable) condition of a flip flop and how can it be eliminated?

8. Compare sequential and combinational circuits.

9. Implement the following Boolean function using ROM $F_1(A_1,A_0) = \sum(1,2)$, $F_2(A_1,A_0) = \sum(0,1,3)$.

10. Classify programmable logic Devices.

Part-B (5 × 10 = 50 Marks)

11. a) Simplify the following Boolean function using Karnaugh map method.   [5]
       $F(A,B,C,D)=\sum(0,1,2,4,5,6,8,9,12,13,14)$.

    b) Obtain the prime implicants for the following Boolean function   [5]
       $F(X,Y,Z)=\sum(01,3,5,7)$.

12. a) Use tabulation method to simplify the given function   [6]
       $F(w,x,y,z))=\sum m(0,1,2,5,7,8,9,10,13,15)$.

    b) Implement the following Boolean function with NAND-NAND logic.   [4]
       $Y=AC+ABC+A^1BC+AB+D$

13. a) Design 8×1 multiplexer using 2×1 multiplexer.   [5]

    b) Implement Half Adder using 4 NAND gates.   [5]

14. a) Design a counter circuit using JK flip flops which counts 0,1,2,4,5,6,0.   [6]

    b) Explain SR Flip-Flop with help of NAND gates also obtain its excitation table.   [4]

15. a) Implement the following two Boolean functions using PLA having three inputs, four   [6]
       product terms and two outputs.
       $F_1(A,B,C)=\sum(0,1,2,4)$
       $F_2(A,B,C)=\sum(0,5,6,7)$.

    b) What is the architectural difference between PROM, PLA and PAL?   [4]

16. a) Simplify the function F(A,B,C,D) = (0,2,6,11,12,13,14) using k-maps and implement the circuit using NAND gate only.   [6]

  b) Implement EX-OR gate using NAND gates and NOR gates.   [4]

17. Answer any *two* of the following:

  a) Design a circuit with four inputs and one output where the output is 1 if the input is divisible by 3 or 7.   [5]

  b) Design a Modulo-7 binary counter using J K Flip-Flop. Draw its state diagram.   [5]

  c) Explain AND-OR structure of PLA & PAL.   [5]

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